MICROMACHINED STIMULATING MICROELECTRODE ARRAYS

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Summary

This contract seeks to develop a family of thin-film stimulating arrays for use in neural prostheses. STIM-2B/-3B are two- and three-dimensional arrays of stimulating sites on 400µm centers. The probes have four channels and 64-sites. Any selected site can be used for either recording or stimulation. Current generation is off-chip. This probe design has now been completed, with 3D arrays of the STIM-3B probes formed in arrays as large as 1024 sites (256 shanks and 64 parallel data channels, accessible over just eleven external leads). The high-end probes STIM-2/-3 are similar except they use on-chip current generation via 8-bit digital to analog converters. They are accessible over seven external leads.

During the past quarter, work under this contract focused on completing the fabrication of the first of the re-designed STIM-2 and STIM-3 stimulating probes and on the development of a wireless interface for them. Test results on test devices from this processing run revealed very good device characteristics, at or near the design specifications. The first STIM-3 probes have been released and are in test. A redesign of the dielectric mask was necessary as part of this release process to ensure that the fold-down ribbon cables on these devices were fully released while the circuit areas was adequately protected. Based on this experience, new probe layout rules were derived to ensure high yield on complex multi-probe wafers. The POR circuits and several others are fully functional on these probes. A higher-than-expected background substrate current is being explored.

Tests on sample devices from these wafers revealed sheet resistances for most of the interconnect layers in the 20-60 ohm/square range, close to target values. Contact resistances are approximately 20Ω, with nMOS thresholds of about 0.7V and pMOS threesholds of about –1.1V. NPN transistor gain is about 100 for the UM 3µm process. Five different rectifier designs were evaluated to determine optimum performance. Breakdown voltages were 22V and 45V, with layout areas from 0.06 to 0.48mm^2. A Zener-referenced open-loop voltage regulator produces a 35mV/V regulation at 340µA in a layout area of 0.73mm^2, while a V_{be}-referenced closed-loop regulator produces a regulation of 47mV/V at 120µA with a layout area of 0.97mm^2. All of this circuit performance is consistent with the formation of a complete telemetry interface for the stimulating probes, and such an interface is now being assembled. Test results are expected during the coming term.

MICROMACHINED STIMULATING MICROELECTRODE ARRAYS

1. Introduction

The goal of this contract is the development of active multi-channel arrays of stimulating electrodes suitable for studies of neural information processing at the cellular level and for a variety of closed-loop neural prostheses. The probes should be able to enter neural tissue with minimal disturbance to the neural networks there and deliver highly-controlled (spatially and temporally) charge waveforms to the tissue on a chronic basis. The probes consist of several thin-film conductors supported on a micromachined silicon substrate and insulated from it and from the surrounding electrolyte by silicon dioxide and silicon nitride dielectric films. The stimulating sites are activated iridium, defined photolithographically using a lift-off process. Passive probes having a variety of site sizes and shank configurations have been fabricated successfully in past contracts and have been distributed to a number of research organizations nationally for evaluation in many different research preparations. For chronic use, the biggest problem associated with these passive stimulating probes concerns their leads, which must interface the probe to the outside world. Even using silicon-substrate ribbon cables, the number of allowable interconnects is necessarily limited, and yet a great many stimulating sites are ultimately desirable in order to achieve high spatial localization of the stimulus currents.

The integration of signal processing electronics on the rear of the probe substrate (creating an "active" probe) allows the use of serial digital input data that can be de-multiplexed on the probe to provide access to a large number of stimulating sites from a very few leads. Our goal in this area is to develop a family of active probes capable of chronic implantation in tissue. For such probes, the digital input data must be translated on the probe into per-channel current amplitudes that are then applied to tissue through the sites. Such probes generally require five external leads, virtually independent of the number of sites used. As discussed in previous reports, we have designed a series of active probes containing CMOS signal processing electronics. Two of these probes have been completed and are designated as STIM-1A and STIM-1B. A third probe, STIM-2, is now beginning a final iteration and is a second-generation version of our original high-end first-generation design, STIM-1. All three probes provide 8-bit resolution in digitally setting the per-channel current amplitudes. STIM-1A and -1B offer a biphasic range using ±5V supplies from 0μA to ±254μA with a resolution of 2μA, while STIM-2 has a range from 0 to ±127μA with a resolution of 1μA. STIM-2 offers the ability to select 8 of 64 electrode sites and to drive these sites independently and in parallel, while STIM-1A allows only 2 of 16 sites to be active at a time (bipolar operation). STIM-IB is a monopolar probe, which allows the user to guide an externally-provided current to any one of 16 sites as selected by the digital input address. The high-end STIM-2 contains provisions for numerous safety checks and for features such as remote impedance testing in addition to its normal operating modes. It also offers the option of being able to record from any one of the selected sites in addition to stimulation. It will be the backbone of a

multi-probe three-dimensional (3D) 1024-site array (STIM-3) now in development. A new probe, STIM-2B, has recently been added to this set. It offers 64-site capability with off-chip generation of the stimulus currents for four separate channels. These channels are organized in four groups so that each current can be directed to any of the 16 sites in its group. Each selected channel can be programmed for either stimulation or recording. On-chip recording amplifiers offer a gain of 50; alternatively, the neural activity can be recorded using off-chip amplifiers interfaced through the normal stimulating channels. This probe is available in both 2D and 3D versions (as STIM-2B/3B) and is now being used in-vivo.

During the past quarter, we have focused work on completing the fabrication of the STIM-2 and STIM-3 probes as well as the realization of the first wireless interface for them. The results of these efforts are described more fully in the sections below.

2. STIM-2/3: A Multiplexed Stimulating Probe with On-Chip Current Generation

As noted during previous quarterly report, we have re-designed our high-end 64-site 8-channel stimulating probes (STIM-2/-3) and have now re-fabricated them as well. The specifications of STIM-2 are repeated below in Table 1 along with the performance specifications for its on-chip recording amplifier. The modified probe has seven external leads (VDD, GND, VSS, CLK, STB, Data In, and (analog) Data Out. It features a new digital-to-analog converter (DAC) with improved performance as well as extensive self-test capabilities to allow the probe to be tested automatically prior to microassembly in 3D arrays (STIM-3). The probe is configured with eight shanks, with the sites spaced at 200µm intervals in depth and the shanks spaced laterally at 400µm. It now contains a significant amount of self-test circuitry so that the probes can be extensively tested at wafer level and individually prior to bonding or insertion into 3D arrays. Figure 1 shows the layout of STIM-3.

During the past quarter, the primary focus of activity was to complete the fabrication and begin testing of the acute and chronic STIM-2/3 probes along with a platform-based interface chip for use with the STIM-3 arrays. As part of the fabrication sequence, the STIM-3 probes offered a special challenge because they are designed to allow the circuit areas to fold down flat against the cortex to minimize the vertical clearance required between the probes and the skull. In the past, it was thought that fabricating silicon ribbon cables on the active probes was difficult or impossible because of the need to etch the cables to a thickness of <5µm while leaving the circuit area backed by 30-40µm of lightly-doped silicon; however, new etching techniques now employed on the probes overcome this problem and still provide a process window consistent with high yield.

In releasing the new fold-down probes from the wafer, it was noted that there was some attack of the circuit area as shown in Fig. 2. The reason for this is noted in Fig. 3. As the release etch proceeds from the front and the back, the front etch stops when it

reaches a complete "V". In areas such as that between the circuit area and the mounting slots for the spacers (highlighted), the etch proceeds to an appreciable depth given by the mask opening divided by the square root of two. When the etch coming from the back of the wafer hits this, relatively rapid etching occurs laterally which immediately begins to undercut the circuit area. In contrast, if the front etch terminates at a shallower depth, the back etch must proceed further before lateral etching occurs and the circuit area is preserved. (If the mask opening is too narrow, then the circuit area must be etched too thin before it is released, causing yield loss because of the vertical back-etch itself). Thus, there is a window of acceptable etch mask widths (about 40-60µm) that will result in well-defined circuit/probe features. This is not a problem but does require attention to probe layout and the gaps between probes. In the present STIM-3 mask steps, an additional rectangle of field oxide was inserted as shown in Fig. 3 to correct the problem noted in Fig. 2.

Table 1: Specifications for STIM-2/-3

Process technology	Bulk micromachined 3um n-epi, p-substrate, p-well CMOS process
Power supplies	Vcc=5V, Vss=-5V, GND=0V
Current range	±127 µA with 1uA resolution
Total circuit area	5.8mm * 2.5mm
Total external leads	7 (Vcc, Vss, GND, Clock, Data_in, Data_out, STB)
Shank dimension	104µm (Width) , 3.3mm(Length)
Shank spacing	400µm
No. of shank	8
No. of sites per shank	8
Site area	1000µm^2
Site spacing	200µm

Gain	40dB
Bandwidth	3.2Hz~14kHz
Power consumption	212.1µW
Input reference noise	7.93µVrms

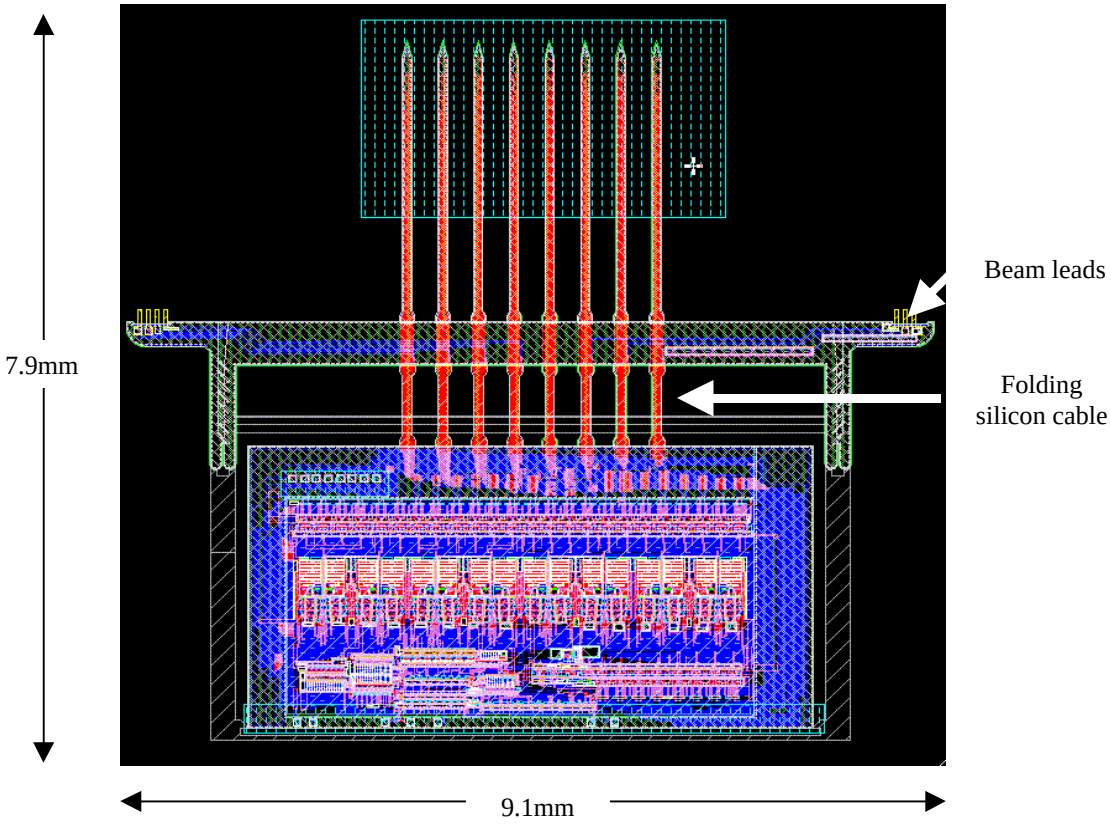


Fig. 1: Layout of STIM-3. The shaded blocks around the probe indicate where dielectric compensation is being used.

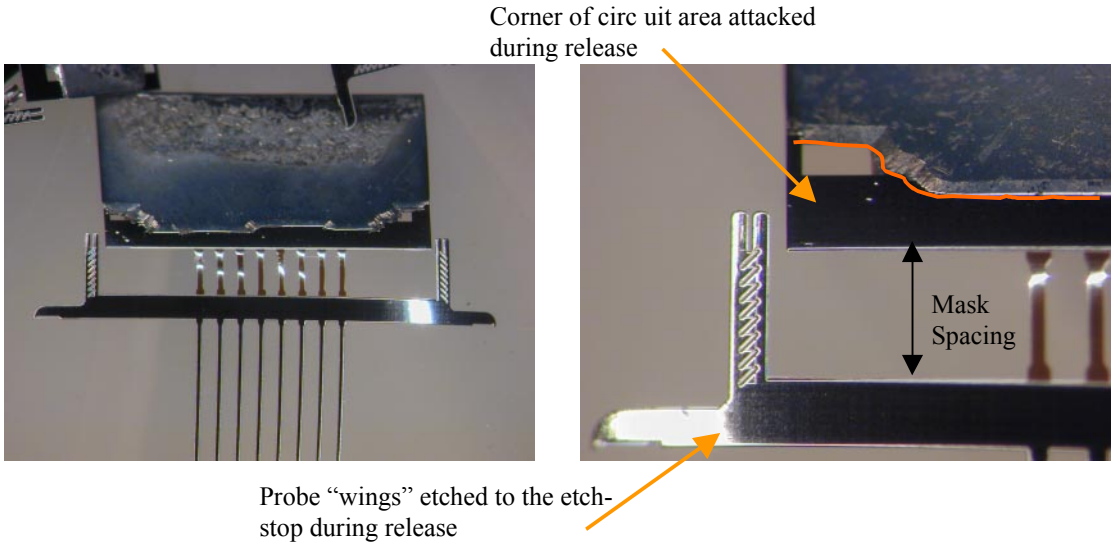


Fig. 2: Released STIM-3 probe with integrated ribbon cables for folding over the circuit. Attack of the circuit area is initiated at the corners of the structure as noted.

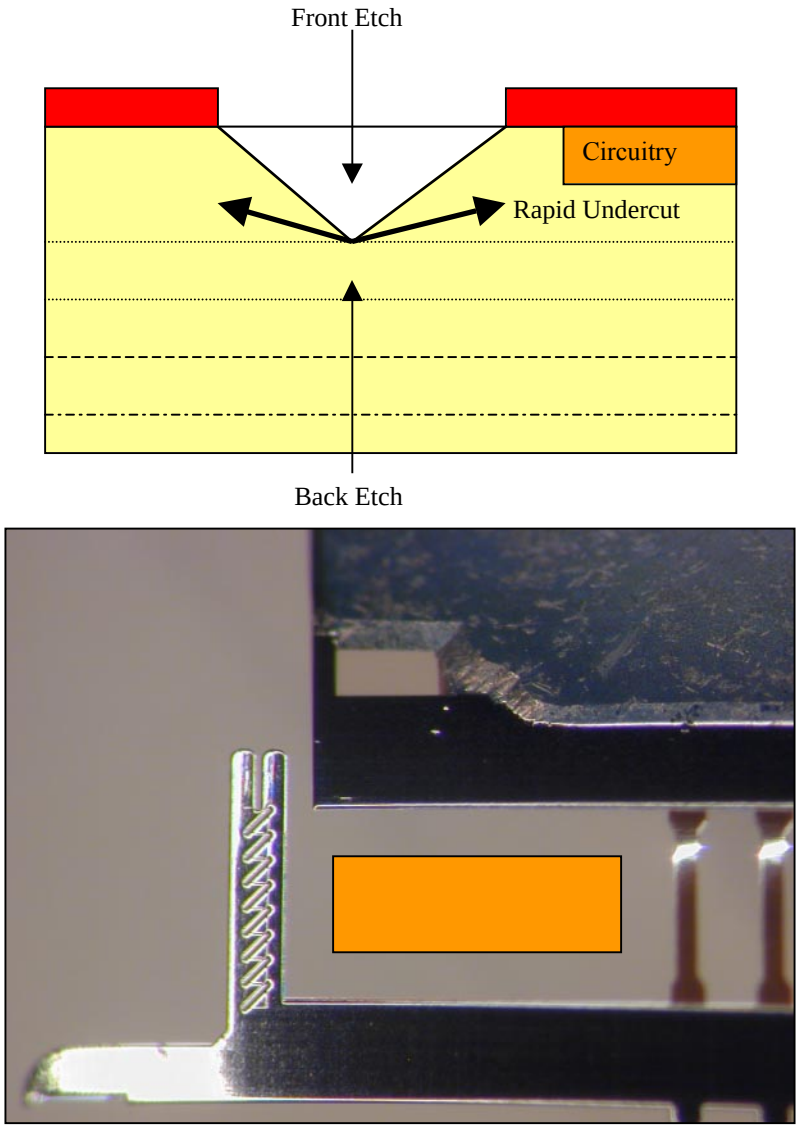


Fig. 3: Illustration of the lateral undercut problem associated with the meeting of the front- and back-etches in releasing a probe (above). Below: Superimposed field dielectric pattern inserted on mask redesign to decrease the mask opening and delay the merging of the etches, preserving the circuit area on subsequent wafers.

Figure 4 shows a test chip that was included on the STIM-2/-3 probe layout to facilitate testing of the various circuit blocks. This includes the on-chip recording amplifier, the input shift register, the power-on-reset circuit, and the current-output digital-to-analog converter. All of these elements are now in test. As will be noted below, the device characteristics on this chip look excellent, indicating that the process went well. Figure 5 shows a detail of the power-on-reset output, which is fully functional. Testing of the other circuit blocks is underway. Figure 6 shows the platform chip. In testing it, a relatively large leakage current has been found, the cause of which is

currently being investigated. We hope to present complete characterization results on these probes in the next report.

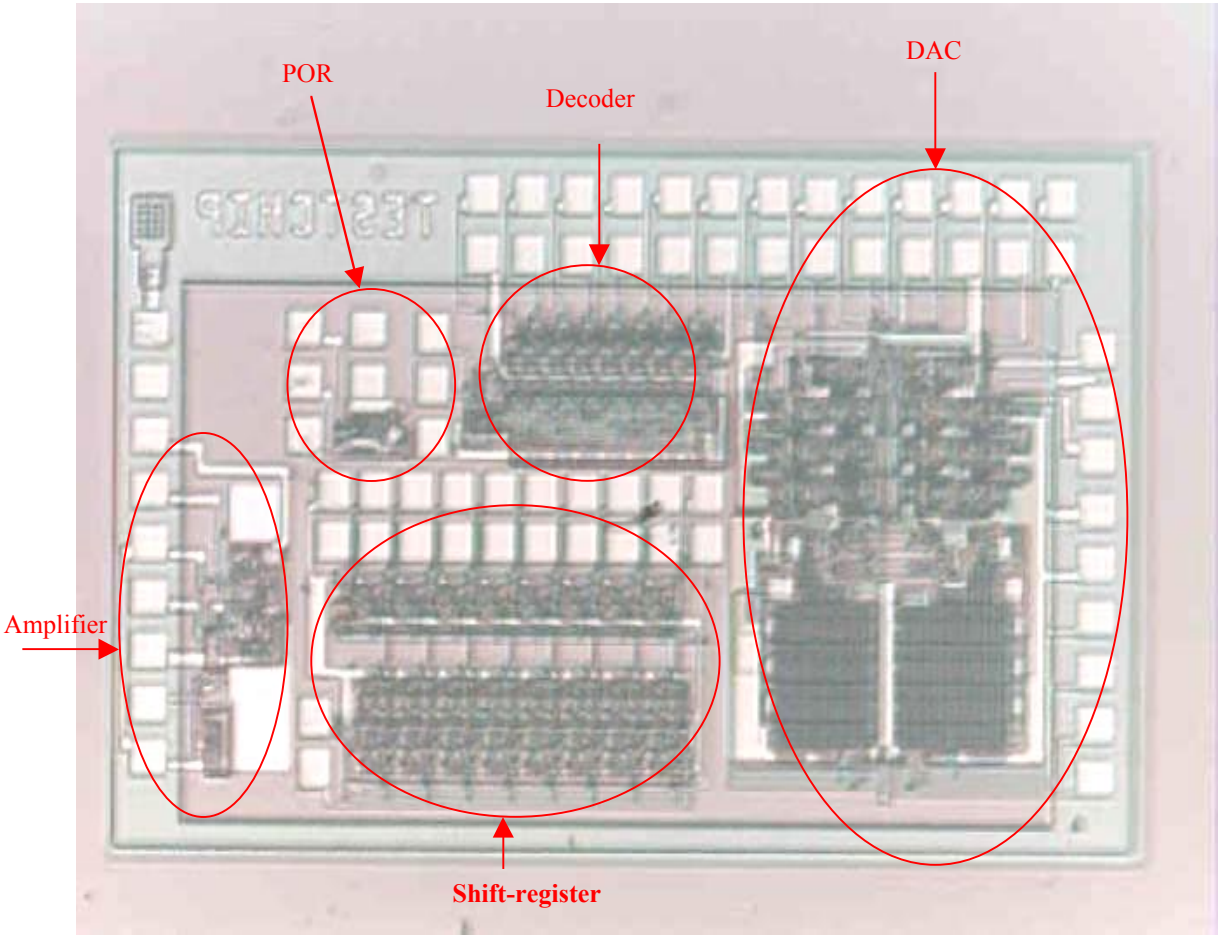


Fig 4: Picture of the testchip on the STIM-2/-3 wafers

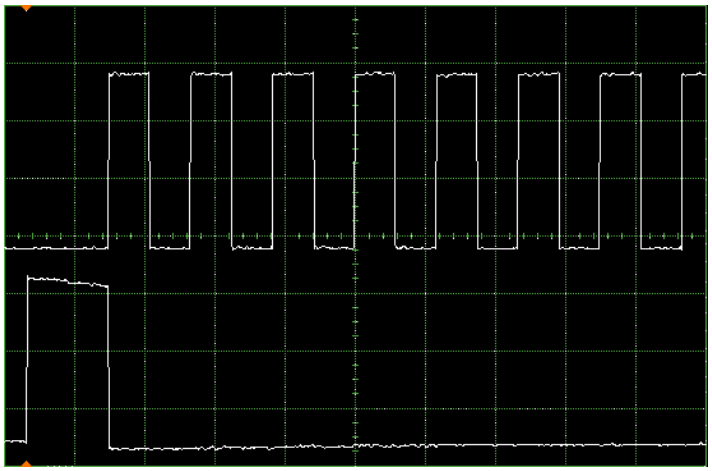


Fig. 5: Waveform of the POR circuitry, top: clock signal, bottom, POR signal

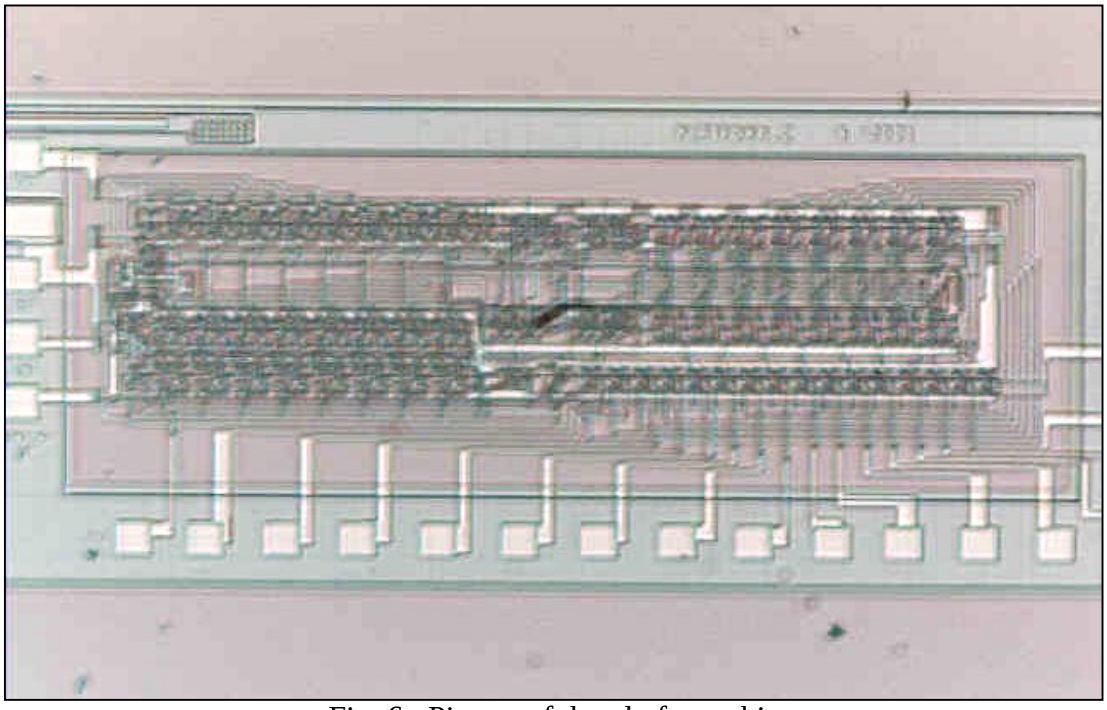


Fig. 6: Picture of the platform chip

3. A Wireless CNS Stimulating System

3.1 A Stand-Alone 4-Channel Wireless Stimulator Chip:

Design of a stand-alone 4-channel wireless stimulator chip, so-called Interestim-2, was completed during the previous quarter (Jul-Sep 2001) and was included in the fabrication mask set. Low-power circuit design techniques were employed in the design of Intersestim-2, which was described in the last quarterly report. This ASIC chip interfaces with passive micromachined stimulating microprobes. The block diagram of Intersestim-2 is shown in Fig. 7.

The University of Michigan's single-metal dual-poly 3µm BiCMOS process run was finished early in this quarter and the remainder of the time was spent on characterization of individual devices and testing of several test structures and different versions of the Interestim chips. These tests are still in progress and we are going to use functional chips in a larger system by putting together different components of a wireless stimulating microsystem such as the transmitter circuitry, receiver/transmitter coils, and a PC-based command generation station. This report summarizes the results of this testing and characterization.

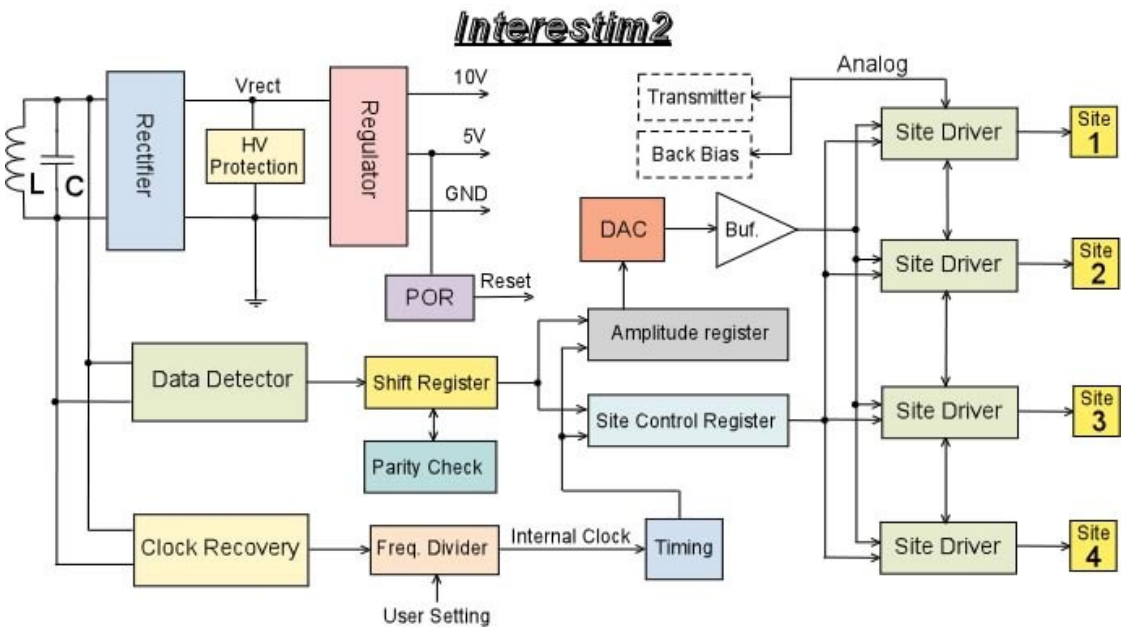


Fig. 7: Interestim-2 block diagram

3.2 Characterizing Individual Devices and Circuit Components

Characterization of the test devices and circuit components was performed on a test-bench and focused on various devices available in the UofM BiCMOS process with different geometries. Most of the parameters varied slightly from one wafer to another or on different spots on a single wafer. Therefore, the range of the parameter variation or an average parameter value is reported.

Sheet Resistance: Table 1 shows some of the measured sheet resistance values from the test structures of different layers. For measuring those that have lower values, such as metal, the 4-point probing method has been used to cancel the effects of probe contact resistance. Almost all the values are close to the expected range except for the metal, which is an order of magnitude more resistive. It turns out that this is because of a change in the aluminum and silicon percentage in the material used for the metal interconnect, which is necessary to ensure high iridium site adhesion in the later steps. Further tests demonstrated that since the metal line width was designed wide enough in the layout for high current lines such as supply rails, the high metal resistivity did not cause any major problems. We also learned that the metal sheet resistance increases slightly after the sintering step.

Contact Resistance: The contact resistance between metal and other layers is usually considered as a parasitic and should not be too high. The values shown in Table 2 have been measured on a test structure with 100 contacts in series to verify the quality of these contacts as well.

TABLE 1
MEASURED SHEET RESISTANCE

Layer	**Sheet Res. Ω**	**Target Ω**
Metal	0.7~2.2	0.1
Poly-1	22.7~27	11
Poly-2	36~42	22
Diffusion-Nplus	20~25	75
Diffusion-Pplus	47~55	120
P-Well	1270~1430	-

TABLE 2
MEASURED CONTACT RESISTANCE

Metal and …	**Contact Res. Ω**	**Target Ω**
Poly-1	20.1	21
Poly-2	25.5	21
Diffusion-Nplus	13.7	29
Diffusion-Pplus	39.1	31

TABLE 3
MOS TRANSISTOR PARAMETERS

Parameter	**Measured Value**	**Target**
V_{th-N}	0.6~0.8 V	0.9 V
$\|V_{th-P}\|$	0.8~1.1 V	0.9 V
K_{p-N}	15.36~32.5 A/V^2	35.6 A/V^2
K_{p-P}	14.5~23.94 A/V^2	17.5 A/V^2
λ_N	0.025~0.054 V^{-1}	<0.019 V^{-1}
λ_P	0.018~0.036 V^{-1}	<0.045 V^{-1}

Capacitors: The dual-poly capacitor values were in the expected range of 0.34 to 0.46 $pF/\mu m^2$.

MOSFETs: NMOS and PMOS transistor curves are shown in Figs. 2 and 3. These tests were performed on transistors with different geometries to study secondary effects such as short channel, narrow channel, and impact ionization effects. Figures 2a and 2b are used to measure MOS threshold voltages while V_{DS} is kept constant at 2V. Based on previous experience in which large threshold voltage shifts had been observed in the UofM process, all circuits were designed to be robust against threshold voltage

variations. However, the threshold voltages were very close to the target values in this run!

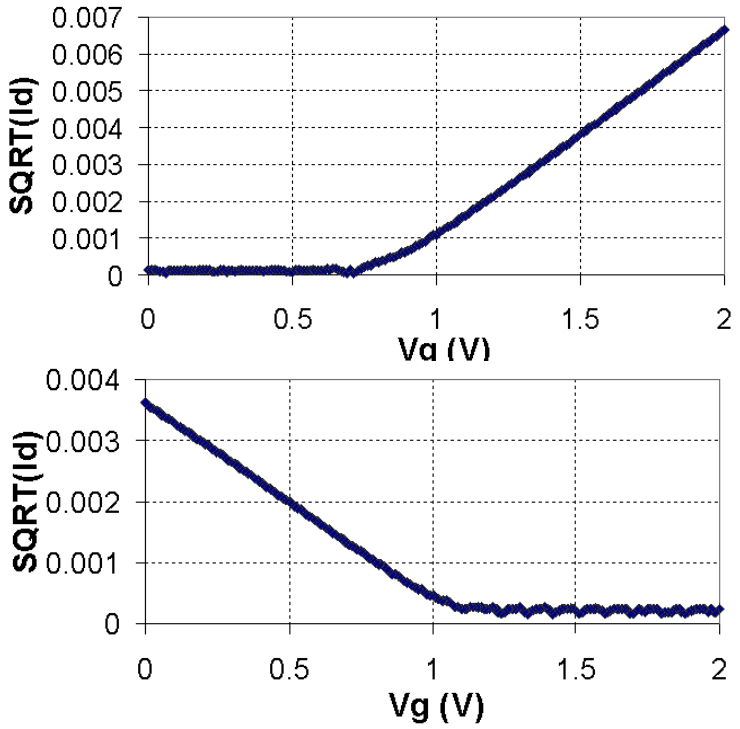


Fig. 8: Minimum size (3x3µm) NMOS and PMOS transistor V_G-SQRT(I_D) curves with V_{DS}=2V

Figure 9 shows I_D-V_{DS} curves for NMOS and PMOS transistors with 2 different geometries: minimum size W/L=3/3 µm and W/L=20/6 µm. $|V_{GS}|$ has been changed in 0.1V steps from 0.5V to 1.4V in NMOS and from 0.6V to 1.5V in PMOS transistor curves. By comparing Figures 3a and 3b with 3c and 3d, it can be seen that NMOS transistors are much more susceptible to impact ionization in high V_{DS} voltages than their PMOS counterparts. In both short (3µm) and long (6µm) channel NMOS transistors, the slope of I_D-V_{DS} curves starts increasing from V_{DS}>6~8V but the slope of I_D-V_{DS} curves in PMOS transistors is constant well above V_{DS}>15V. This result is supported by semiconductor theory, considering that the impact ionization is much more associated with hot electrons than energetic holes. This is a very important matter in the design of stimulating current sources, because we want to produce constant stimulating current irrespective of the stimulating site voltage. On the other hand, up to 10V of output voltage compliance has been included in our stimulators specifications. Therefore, it can be concluded that the NMOS transistors are not good candidates for the stimulating current source output stages unless they are well compensated for the current changes due to output voltage variations.

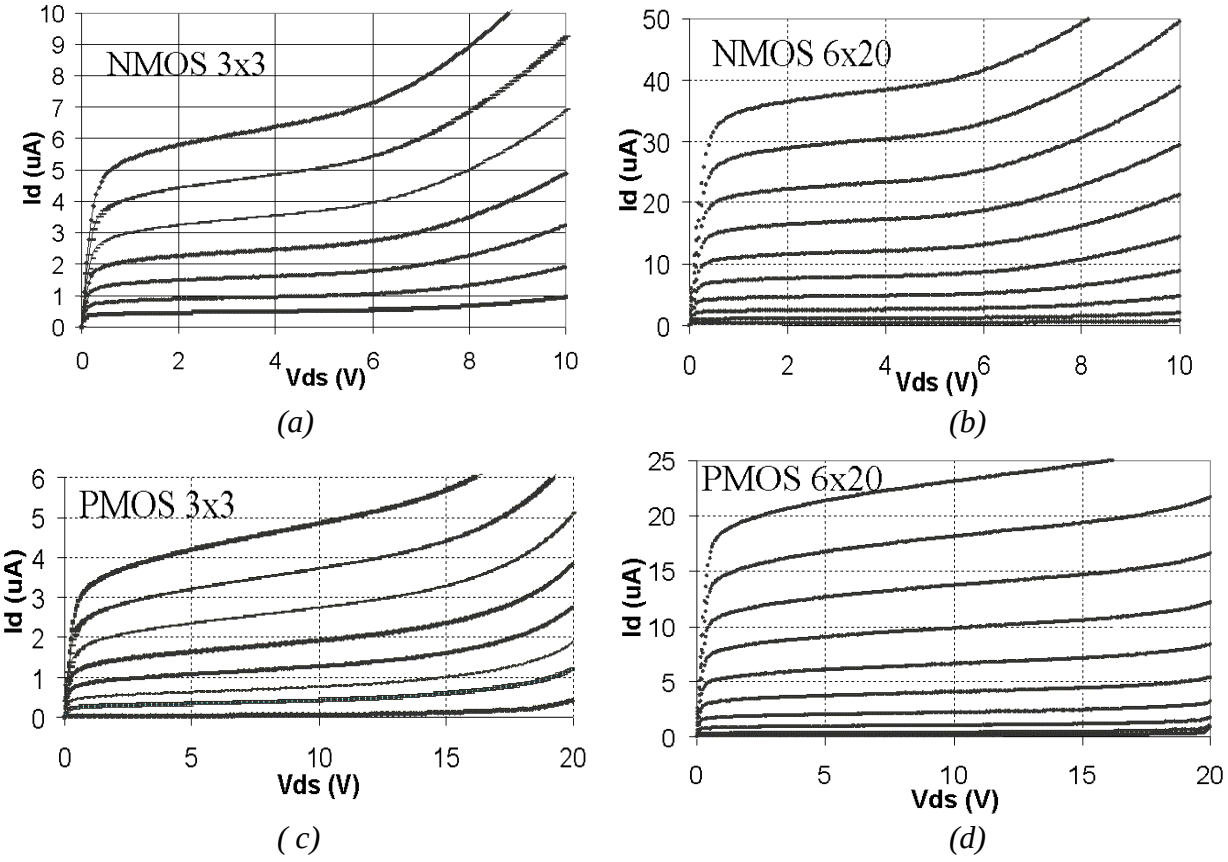


Fig. 9: NMOS and PMOS transistor I_D-V_{DS} curves (a) NMOS, W/L=3/3µm, V_{GS}=0.5~1.4V (b) NMOS, W/L=20/6µm, V_{GS}=0.5~1.4V (c) PMOS, W/L=3/3µm, $|V_{GS}|$=0.6~1.5V (d) PMOS, W/L=20/6µm, $|V_{GS}|$=0.6~1.5V

Many of the MOS transistor parameters can be derived from I_D-V_{DS} curves in Fig. 9, some of which are summarized above in Table 3. Variations in K_P and λ parameters are mostly because of the changes in geometry. It should be mentioned that the target values are only those parameter values, which have been measured from previous runs and are not necessarily the optimum values. For example, we would like to have smaller λ_N and λ_P to increase the transistor output resistance.

BJTs: Past experiments have shown that lateral PNP transistors have poor performance in this process compared to the NPN transistors, which can be implemented in a vertical structure. Therefore, use of the PNP transistors was eliminated in our designs and wherever needed, they were replaced by their PMOS-NPN counterparts. Figure 10a shows the V_{CE}-I_C curves of a minimum size NPN, which has an emitter size of 37µmx7µm. In these curves I_B has been changed from 10µA to 100µA in 10µA steps. Fig. 10b shows the I_B-β curve for the minimum size BJT in the same range of I_B as 10a

when V_{CE} is constant at 4V. The NPN current gain is around 100, which is enough for our purposes.

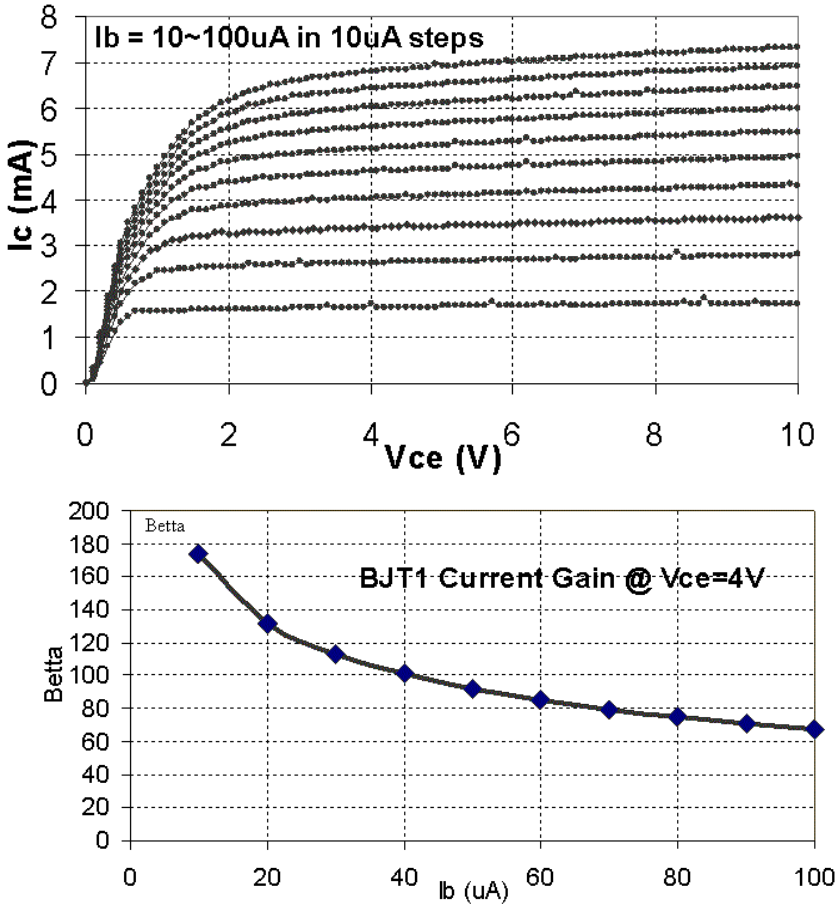


Fig. 10: Minimum size (37x7µm emitter area) NPN transistor (a-above) V_{CE}-I_C curves V_G-SQRT(I_D) curves with I_B=10~100µA in 10µA steps; (b-below) I_B-β curve with V_{CE}=4V.

One major difference between the UofM and standard BiCMOS processes is the lack of a buried layer, which deteriorates the performance of our NPN devices. The NPN transistors are mostly used in diode-connected topology as fully integrated rectifier diodes in the Interestim designs. Figure 11 shows cross-section of a diode-connected NPN transistor with its associated parasitic components. Here, N-epi and P-well are shorted to prevent the parasitic PNP transistor from turning on. However, when the diode is forward biased, current passes through P-well and turns the original NPN on. This in turn passes some of the diode forward current trough the N-epi, which has a high resistivity under the P-well region because of the lack of an n^+ buried layer in this process. If the voltage drop across the N-epi resistor exceeds $|V_{BE(ON)}|$, the parasitic PNP transistor turns on, resulting in current leakage from P-well to the grounded P-substrate. Increasing the rectifier diode area and proper layout have eliminated this effect in normal operating current levels by decreasing the N-epi resistance.

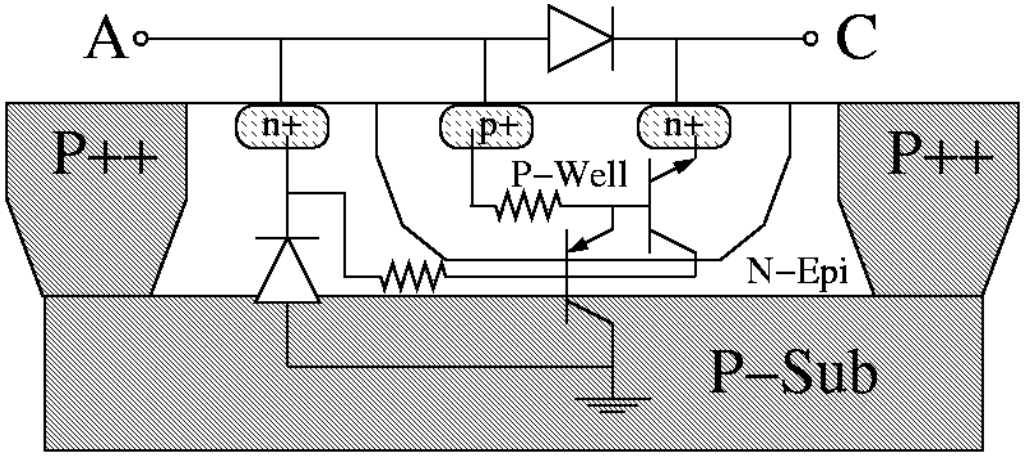


Fig. 11: Cross-section of a diode-connected NPN transistor with its parasitics

Figure 12 shows the diode-connected NPN transistor forward and reversed bias I_D-V_D curves. Diode 7 is the same as Diode 1 with 7 times higher emitter area for passing larger amount of current in rectifiers without turning on the parasitic PNP. However, the diode high frequency performance should be compromised because of the increased parasitic capacitors. The diode-connected NPN reverse breakdown voltage is another important parameter, which is shown in Fig. 12b. These diodes are directly connected to the receiving coil and should survive large voltage swings. Table 4 summarizes some of the NPN transistor characteristics.

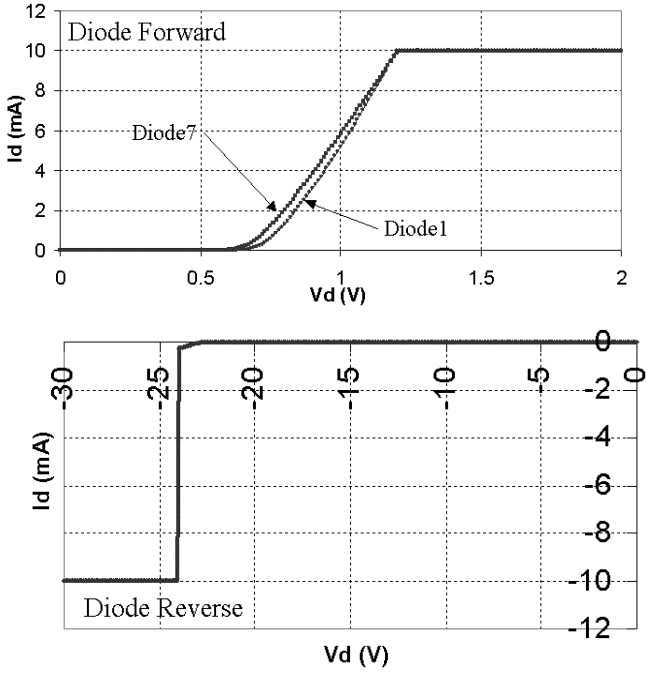


Fig. 12: Diode-connected NPN transistor forward and reversed bias I_D-V_D curves. (a) above; (b) below

Zener Diodes: Zener diodes have been used as voltage reference and protection against high input voltage in design of the Interestim circuits. Fig. 13 shows the measured characteristic curves of two different diode designs, called *zen1* and *zen5*, which have been described in previous reports. *zen5* has a larger geometry and conducts more strongly in forward bias (Fig. 13a). In the reverse bias, as shown in Fig. 13b, *zen5* has a sharper knee-point and about 3 times more current conduction after Zener breakdown. This is shown in Fig. 13c by differentiating the reverse biased I_D-V_D curves, which means that *zen5* is a better choice for voltage reference as well as high voltage protection. However, *zen1* is more attractive for very low power circuits because it needs less biasing current to pass the knee-point. The breakdown voltages in different wafers were in the 5.2~5.4V range.

TABLE 4
NPN TRANSISTOR PARAMETERS

Parameter	**Measured Value**	**Target**
β_F	65-175	200
Va	81.8~84.6 V	>50 V
I_s	0.5~0.8 fA	<5 fA
Emitter Area	7x37 μm^2	7x37 μm^2
Diode Bereakdown	22.5~25 V	>23 V

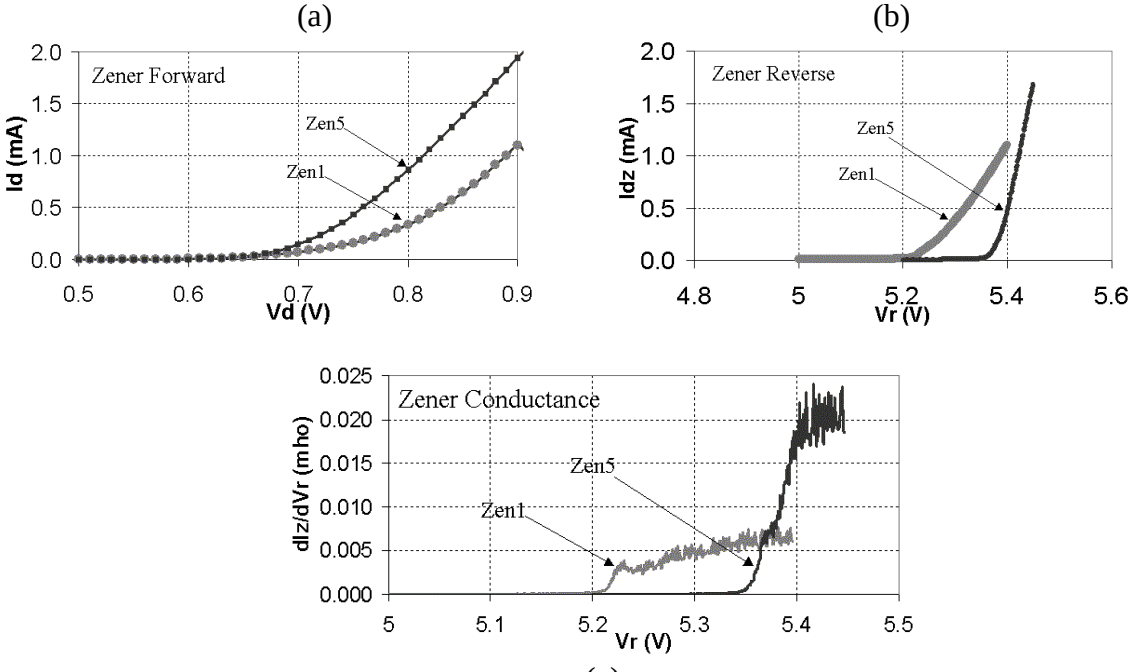


Fig. 13: Zener diode (a) forward bias I_D-V_D curves (b) reversed bias I_D-V_D curves (c) conductance in reverse bias

3.3. Testing Individual blocks:

Several test-chips including different versions of the individual block have been designed and implemented. These individual blocks were laid out with cutting links in order to change some critical component values after fabrication in actual measurements to discover the best designs and parameter values for future system developments.

Rectifier Block: A variety of on-chip rectifier designs, shown in Fig. 14, with different voltage and current handling capabilities were tested on a rectifier test structure. In terms of maximum input voltage, designs A, B, and C, which have a single diode in each branch, cannot handle more than 22V peak-to-peak input voltage because of the NPN-diode reverse breakdown (Fig. 12b). Therefore, considering safety margins, these rectifiers are not suitable for 10V regulators, which need a minimum of 12V unregulated DC input. Designs D and E have two series diodes in each branch and their reverse breakdown goes beyond 40V as shown in Fig. 15. The disadvantage of the 8 diode full-wave rectifier bridge in design E is its large area consumption, but in design D the required area is reduced by 50% by using the parasitic N-epi_P-sub diodes for the returning current path. Reducing the rectifier area also reduces the parasitic capacitors and improves their high frequency performance. All of these designs were implemented in a 2mm x 2mm rectifier test structure, shown in Fig. 16, in two groups with different sizes for diodes, one with minimum size diodes and the other with diodes 10 times larger than the minimum size to test the effect of rectifier diode size on resistive and capacitive parasitic components and the overall performance of different rectifier topologies.

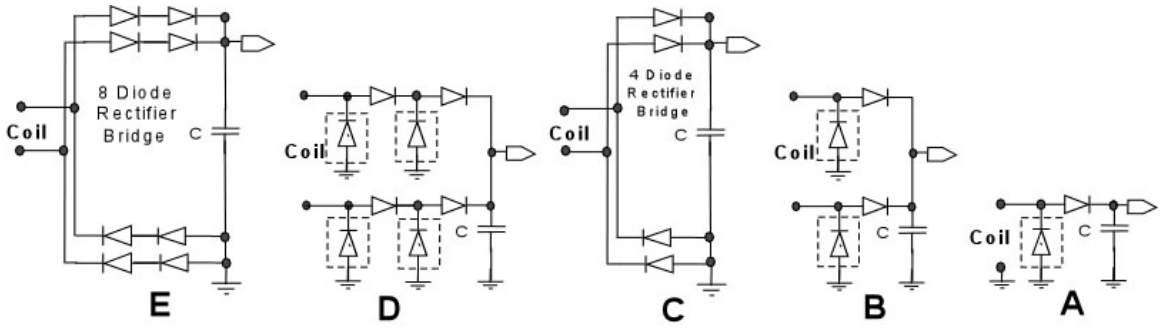


Fig. 14: Different rectifier designs

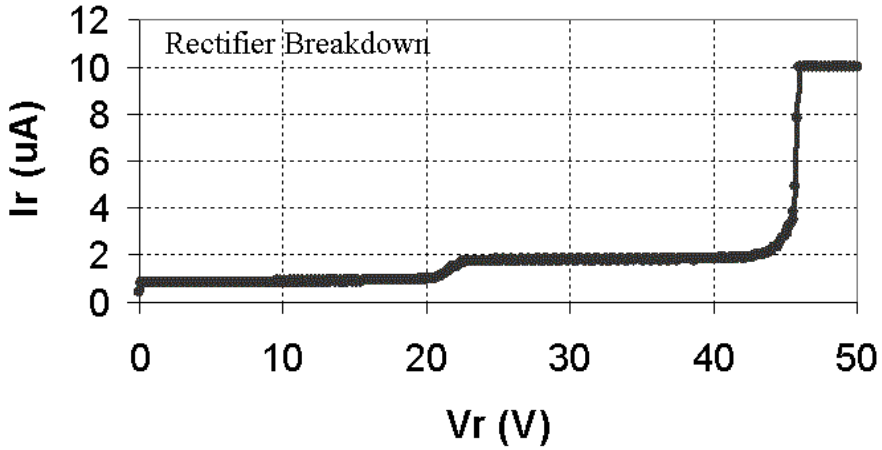


Fig. 15: Full-bridge 8-diode rectifier (E) reverse breakdown.

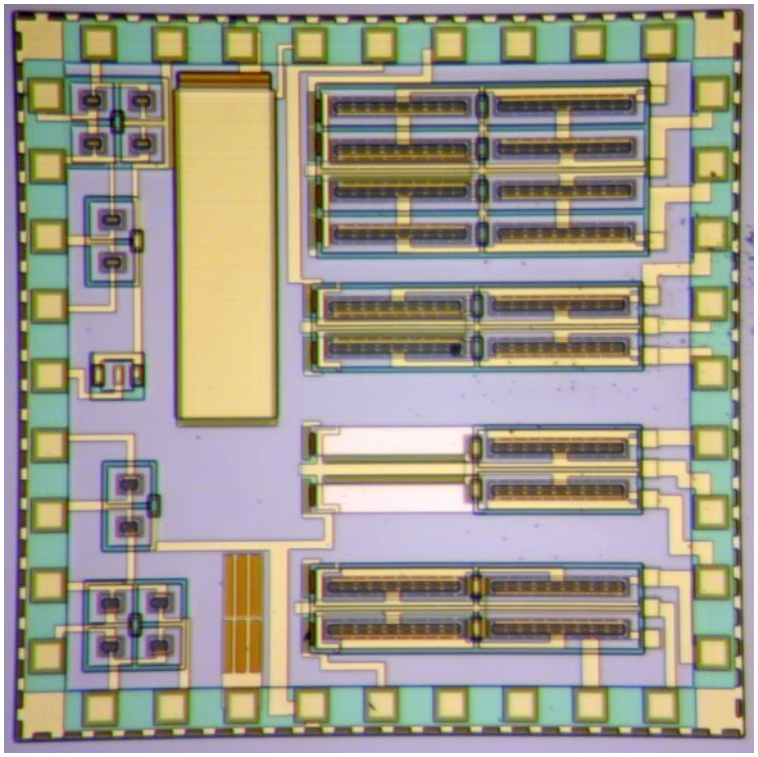


Fig. 16: Rectifier test structure photomicrograph

The frequency responses of the rectifiers C and D have been compared in Fig. 17, which shows the average current passing through a 1kΩ load at different frequencies when the sinusoidal input voltage has been constant. Rectifier D10, which has Fig. 14D topology and diodes 10 times larger than minimum size, has the best performance at low frequency (100kHz) because of its lowers resistive voltage drop. However, at high frequency (4MHz) rectifier C1, which has Fig. 14C topology and minimum size diodes shows the best performance because of its lower parasitic capacitance. Therefore, for each rectifier

topology, a compromise should be made between parasitic resistance and parasitic capacitance in choosing size of the diodes, based on the operating frequency and maximum current of the rectifier to eliminate both current leakage and high frequency voltage drop. A sample measured full-wave rectifier input and output waveform is shown in Fig. 18. Table 5 summarizes some of the specifications of various rectifier topologies shown in Fig. 14.

TABLE 5
SPECIFICATIONS OF VARIOUS RECTIFIER DESIGNS

Rectifier	**Type**	**Process**	**Area** mm²	**Breakdown** V	**Comment**
A: 1 Diode	Half Wave	3µm UM-BiCMOS	0.06	22	N_epi – P_diff diode
B: 2 Diode	Full Wave	3µm UM-BiCMOS	0.12	22	Using parasitic diodes for returni
C: 4 Diode	Full Wave	3µm UM-BiCMOS	0.24	22	Conventional full bridge
D: 4 Diode	Full Wave	3µm UM-BiCMOS	0.24	45	Same as B with 2 diodes in series
E: 8 Diode	Full Wave	3µm UM-BiCMOS	0.48	45	Same as D with 2 diodes in series

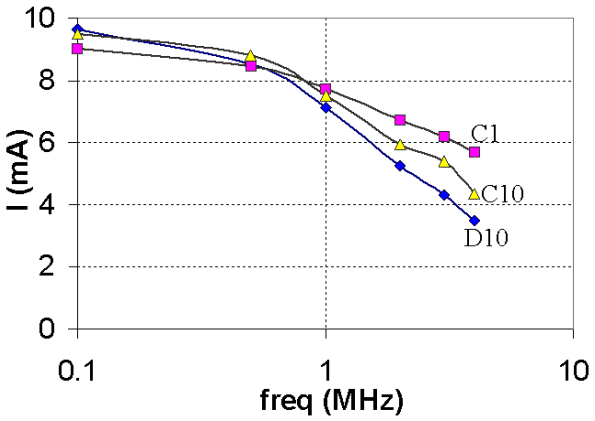


Fig. 17: Rectifier frequency responses.

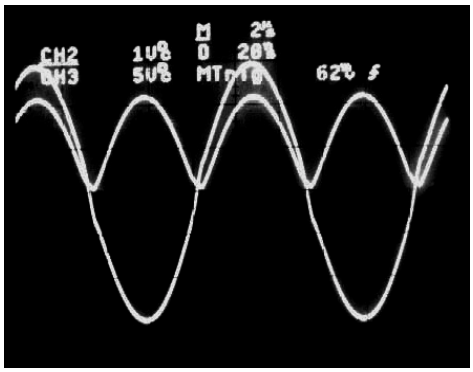


Fig. 18: Measured full-wave rectifier input and output waveforms.

Zener-Referenced Open-Loop Regulator: Several regulator designs in two major categories of open-loop and closed-loop regulators were implemented in a regulator test structure, which is shown in Fig. 20 and tested to find the best fit for this block in the wireless microsystem. Fig. 19 shows a simplified schematic diagram of the Zener-referenced open-loop voltage regulator block. It generates 5V/10V outputs and is able to supply over 10mA from its 10V output. A V_{BE} referenced current source (I_{ref}) is mirrored to bias two 5.4V Zener diodes, which generate 5.4V and 12.2V reference voltages for the unity-gain buffer and a Darlington pair pass transistor pair respectively. The extra 0.4V of reference voltages presumably compensates for the voltage drop caused by the pass transistor parasitic resistors shown in Fig. 11. According to Fig. 13b, the Zener diode *Zen5* needs a minimum of 70µA to pass its knee-point and the current source needs less

than 15µA. Therefore, based on the simulation results the regulator internal current consumption, excluding the unity-gain buffer, is kept below 100µA.

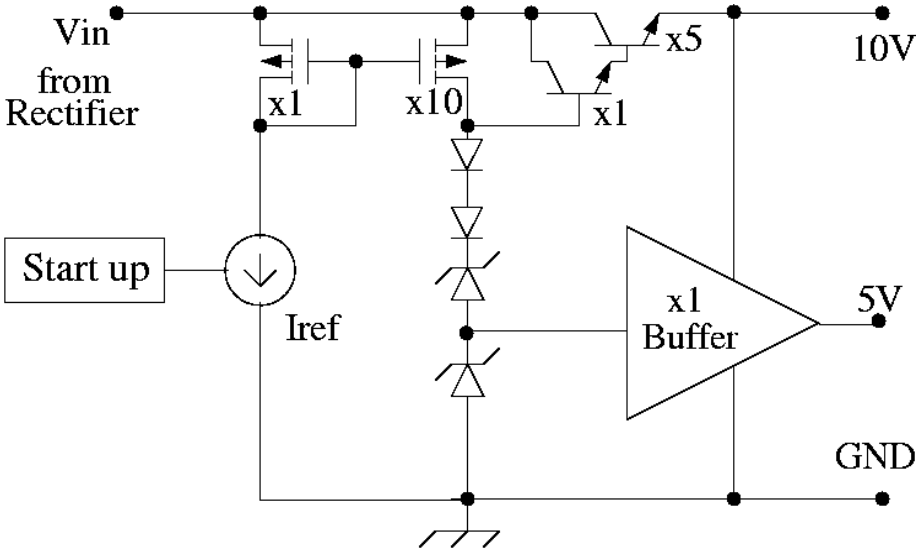


Fig. 19: Simplified schematic diagram of the Zener-referenced open-loop dual-output voltage regulator block.

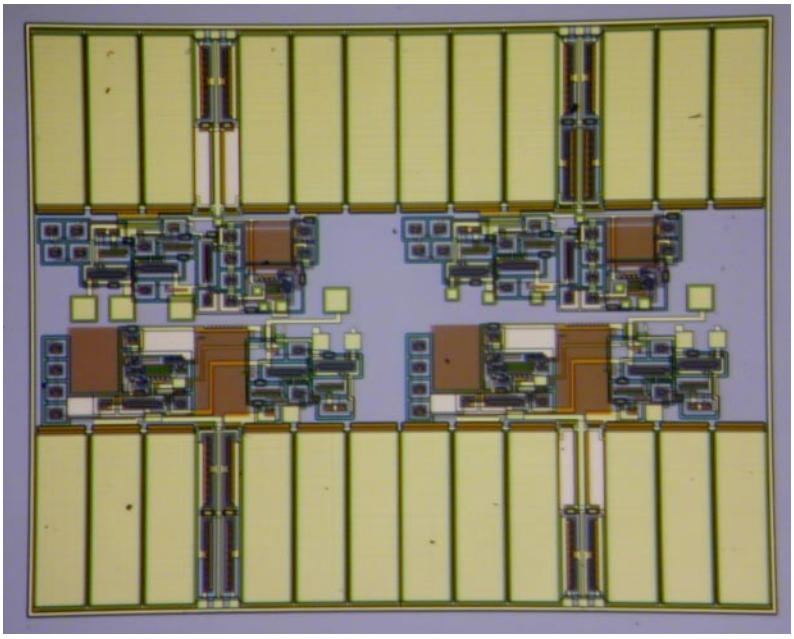
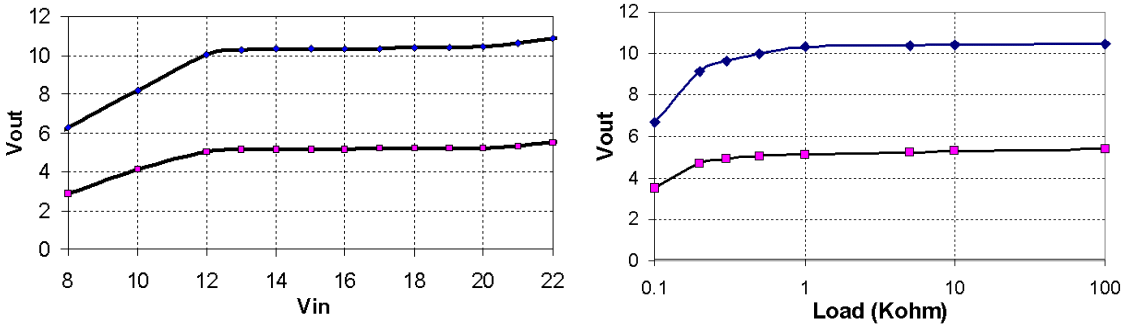
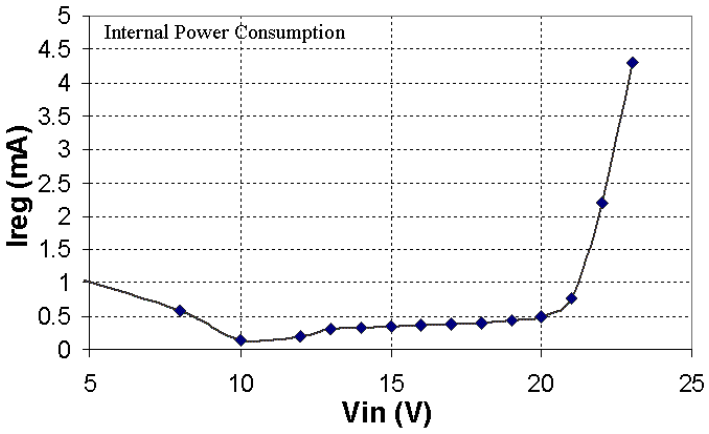


Fig. 20: Regulator test structure photomicrograph

Figure 21 shows the performance measures of the dual-output open-loop voltage regulator. Regulation starts from 12.5V minimum DC voltage at the input. For the input voltage range of 13V-20V, the line regulation in Fig. 21a is better than 35mV/V on both 5V and 10V outputs with 1kΩ loading. The load regulation curves in Fig. 21b show that the regulator can give as much as 10mA with only 0.3V drop when the input is kept constant at 15V. Fig. 21c shows the open-loop regulator internal current consumption including the unity-gain buffer. This current varies from 300µA to 450µA in the nominal input range and its value at 15V DC input is 340µA. Fig. 22a shows a sample measured 4MHz rectified input signal and the regulated DC output waveforms. Fig. 22b shows the AC ripple components at 8MHz on the full-wave rectified input, 10V output, and 5V output from top to bottom. It can be seen that the regulator ripple rejection is higher than 22dB with 1kΩ loads connected between 10V-5V and 5V-GND outputs in Fig. 19. The high frequency ripple rejection is more critical in recording neural signals, but since the neural tissue is not sensitive to MHz frequency range, this amount of ripple rejection should be good enough for this application.

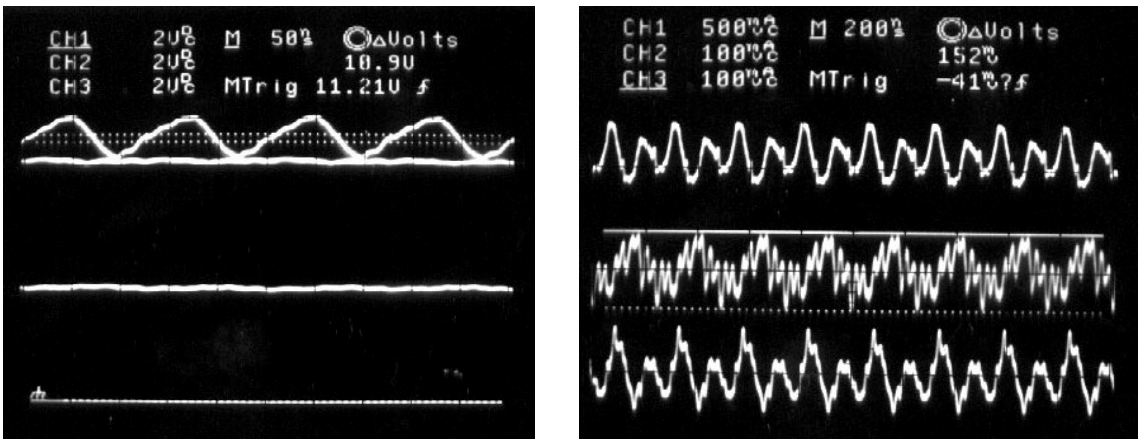


((a) (b)



(c)

Fig. 21: (a) Dual-output open-loop voltage regulator line regulation with 1KΩ loads; (b) Regulator load regulation with 15V DC input; (c) Regulator internal current consumption including the unity-gain buffer.



(a) (b)

Fig. 22: Sample measured waveforms (a) Unregulated DC input and regulated DC output waveforms (b) input and output ripple at 4MHz.

V_{be} Referenced Closed-Loop Regulator: Fig. 23 shows a simplified schematic diagram of the Zener-referenced open-loop voltage regulator block. It generates 5V/10V outputs and is able to supply over 10mA from its 10V output. A V_{be} referenced current source generates all of the required reference voltage and currents in this regulator. A fraction (1/16) of the 10V output (0.625V) is compared with the reference V_{be}, which is used for the I_{ref} current source as well. The amplified error signal drives the Darlington-pair pass transistor and stabilizes the output at 10V by means of the negative feedback. The 5V output is taken from the same voltage divider, which is used for the negative feedback. This voltage is then buffered with a unity-gain buffer to be able to source and sink as much as 5mA.

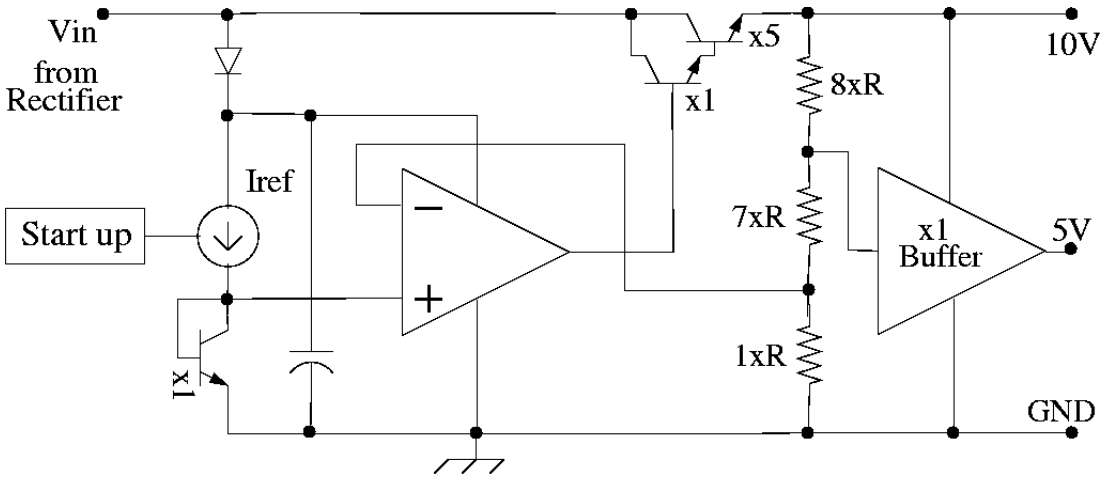
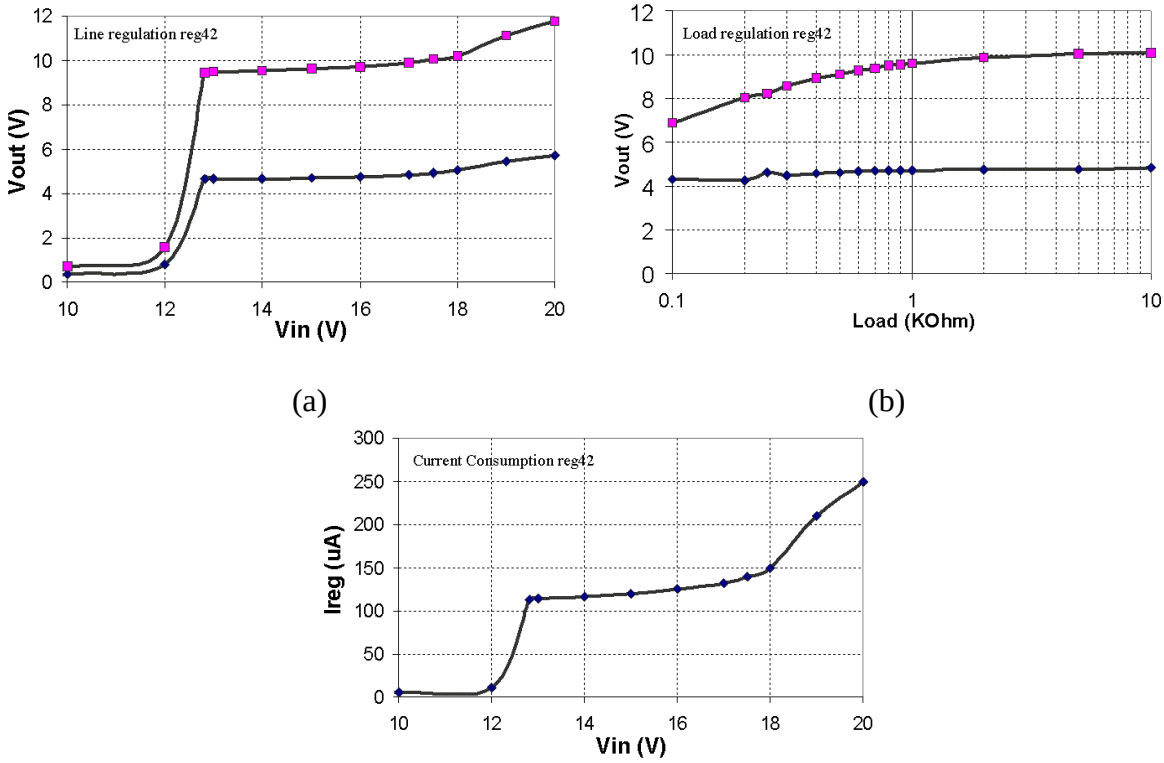


Fig. 23: Simplified schematic diagram of the V_{be} referenced closed-loop dual-output voltage regulator block

Fig. 24a shows the closed-loop regulator line regulation. Regulation starts at 12.8V when the start-up circuit turns on the V_{be} referenced current source. The exact output

voltages can be adjusted after fabrication by changing the resistive voltage divider ratios by cutting links. The 10V and 5V line regulations in the input voltage range of 13V~17V are 95mV/V and 47mV/V respectively, both of them inferior to the open-loop regulator performance in Fig. 21a. However, the load regulation and power consumption are better as shown in Figures 24b and 24c respectively. For a 15V DC input, current consumption is 120µA including the unity-gain buffer. It can be concluded that the open-loop regulator is more suitable where lower ripple and better regulation is needed but the closed-loop regulator is a better choice for low-power designs. Table 6 compares some of the specifications of these two regulator designs.

During the next quarter we will continue testing the individual blocks as well as the complete Interestim-1 and Interestim-2 systems. We are going to work on the transmitter and the PC-based command generator to implement a true wireless stimulating setup for testing the functionality of our chips in vitro.



(a) (b)

(c)

Fig. 18: (a) Dual-output closed-loop voltage regulator line regulation with 1KΩ loads; (b) Regulator load regulation with 15V DC input; (c) Regulator internal current consumption including the unity-gain buffer

TABLE 6
REGULATOR DESIGNS SPECIFICATIONS

Regulator	**Type**	**Process**	**Area** mm^2	**Current Consumption** µA	**5V Line Reg.** mV/V	**10V L Reg.** r
Zener Referenced	Open-loop	3µm UM-BiCMOS	0.73	340 @ 15V input	35	35
V_{be} Referenced	Closed-loop	3µm UM-BiCMOS	0.97	120 @ 15V input	47	95

4. Conclusions

During the past quarter, work under this contract focused on completing the fabrication of the first of the re-designed STIM-2 and STIM-3 stimulating probes and on the development of a wireless interface for them. Test results on test devices from this processing run revealed very good device characteristics, at or near the design specifications. The first STIM-3 probes have been released and are in test. A redesign of the dielectric mask was necessary as part of this release process to ensure that the fold-down ribbon cables on these devices were fully released while the circuit areas was adequately protected. Based on this experience, new probe layout rules were derived to ensure high yield on complex multi-probe wafers. The POR circuits and several others are fully functional on these probes. A higher-than-expected background substrate current is being explored.

Tests on sample devices from these wafers revealed sheet resistances for most of the interconnect layers in the 20-60 ohm/square range, close to target values. Contact resistances are approximately 20Ω, with nMOS thresholds of about 0.7V and pMOS threesholds of about –1.1V. NPN transistor gain is about 100 for the UM 3µm process. Five different rectifier designs were evaluated to determine optimum performance. Breakdown voltages were 22V and 45V, with layout areas from 0.06 to 0.48mm^2. A Zener-referenced open-loop voltage regulator produces a 35mV/V regulation at 340µA in a layout area of 0.73mm^2, while a V_{be}-referenced closed-loop regulator produces a regulation of 47mV/V at 120µA with a layout area of 0.97mm^2. All of this circuit performance is consistent with the formation of a complete telemetry interface for the stimulating probes, and such an interface is now being assembled. Test results are expected during the coming term.